WHAT IS CLAIMED IS:

1. A power MOSFET, comprising:

a low resistive semiconductor substrate of a first conductivity type having a first main surface and a second main surface opposing to each other;

a drift layer of the first conductivity type formed on the first main surface of the semiconductor substrate;

a high resistive epitaxial layer of the first conductivity type formed on the drift layer;

trenches formed in the epitaxial layer and the drift layer to extend from a surface of the epitaxial layer into the drift layer;

gate electrodes buried in the trenches with gate insulating films interposed between walls of the trenches and the gate electrodes;

low resistive source layers of the first conductivity type formed in a surface region of the epitaxial layer adjacent to the gate insulating films;

a base layer of a second conductivity type formed in the surface region of the epitaxial layer;

a source electrode electrically connected to the source layers and the base layer; and

a drain electrode electrically connected to the second main surface of the semiconductor substrate, wherein

the epitaxial layer intervening between

the trenches is depleted in a case where no voltage is applied between the source electrode and the gate electrodes.

2. The power MOSFET according to claim 1, wherein the semiconductor substrate is a silicon substrate, and

the drift layer is formed to satisfy a relational expression: $t < VB/3 \times 10^5$ V/cm,

where the thickness of the drift layer is t, a breakdown voltage of the power MOSFET is VB, and breakdown critical electric field of silicon is 3×10^5 V/cm.

3. The power MOSFET according to claim 1, wherein a width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

4. The power MOSFET according to claim 2, wherein the width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

5. The power MOSFET according to claim 1, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

6. The power MOSFET according to claim 2, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

7. The power MOSFET according to claim 3, wherein

an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

8. The power MOSFET according to claim 4, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

9. The power MOSFET according to claim 1, wherein the trenches are formed to extend from the surface of the epitaxial layer to the semiconductor substrate.

10. A power MOSFET, comprising:

a low resistive semiconductor substrate of a first conductivity type having a first main surface and a second main surface opposing to each other;

a high resistive epitaxial layer of the first conductivity type formed on the first main surface of the semiconductor substrate;

trenches formed to extend from a surface of the epitaxial layer to the semiconductor substrate;

gate electrodes buried in the trenches with gate insulating films interposed between the gate electrodes and walls of the trenches;

low resistive source layers of the first conductivity type formed in a surface region of the epitaxial layer adjacent to the gate insulating films;

a base layer of a second conductivity type formed in the surface region of the epitaxial layer;

a source electrode electrically connected to the source layer and the base layer; and

a drain layer electrically connected to the second main surface of the semiconductor substrate, wherein

the epitaxial layer intervening between the trenches is in a state of being depleted in a case where 0 volt is applied between the source electrode and the gate electrodes.

11. The power MOSFET according to claim 10, wherein a width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

12. The power MOSFET according to claim 10, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

13. The power MOSFET according to claim 11, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

14. A power MOSFET, comprising:

a low resistive semiconductor substrate of a first conductivity type having a first main surface and a second main surface opposing to each other;

a drift layer of the first conductivity type formed on the first main surface of the semiconductor substrate;

a high resistive epitaxial layer of the first

conductivity type formed on the drift layer;

trenches formed to extend from a surface of the epitaxial layer into the semiconductor substrate;

gate electrodes buried in the trenches with gate insulating films interposed between the gate electrodes and walls of the trenches;

low resistive source layers of the first conductivity type formed in a surface region of the epitaxial layer adjacent to the gate insulating films;

a base layer of a second conductivity type formed in the surface region of the epitaxial layer;

a source electrode electrically connected to the source layers and the base layer; and

a drain electrode electrically connected to the second main surface of the semiconductor substrate, wherein

the epitaxial layer intervening between the trenches is depleted in a case where 0 volt is applied between the source electrode and the gate electrodes, and the thickness of a part in the gate insulating films corresponding to the epitaxial layer is thinner than the other parts thereof.

15. The power MOSFET according to claim 14, wherein an impurity concentration of the drift layer on a side of the drain electrode is higher than that of a side of the source electrode.

16. The power MOSFET according to claim 14,

wherein the impurity concentration of the drift layer is $1 \times 10^{16}/cm^3$ to $7 \times 10^{16}/cm^3$ on the side of the source electrode, and $1 \times 10^{17}/cm^3$ to $3 \times 10^{17}/cm^3$ on the side of the drain electrode.

17. The power MOSFET according to claim 14, wherein

the semiconductor substrate is a silicon substrate, and

the drift layer is formed to satisfy a relational expression: $t < VB/3 \times 10^5$ V/cm,

where the thickness of the drift layer is t, a breakdown voltage of the power MOSFET is VB, and a breakdown critical electric field of silicon is 3×10^5 V/cm.

18. The power MOSFET according to claim 15, wherein

the semiconductor substrate is a silicon substrate, and

the drift layer is formed to satisfy a relational expression: $t < VB/3 \times 10^5$ V/cm,

where the thickness of the drift layer is t, a breakdown voltage of the power MOSFET is VB, and a breakdown critical electric field of silicon is 3×10^5 V/cm.

19. The power MOSFET according to claim 16, wherein

the semiconductor substrate is a silicon

substrate, and

the drift layer is formed to satisfy a relational expression: $t < VB/3 \times 10^5$ V/cm,

where the thickness of the drift layer is t, a breakdown voltage of the power MOSFET is VB, and a breakdown critical electric field of silicon is 3×10^5 V/cm.

20. The power MOSFET according to claim 14, wherein a width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

21. The power MOSFET according to claim 15, wherein a width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

22. The power MOSFET according to claim 16, wherein a width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

23. The power MOSFET according to claim 17, wherein a width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

24. The power MOSFET according to claim 18, wherein a width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

25. The power MOSFET according to claim 19, wherein a width of the epitaxial layer intervening between the trenches is set at 0.8 μm or less.

26. The power MOSFET according to claim 14, wherein an impurity concentration of the epitaxial

layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

27. The power MOSFET according to claim 15, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

28. The power MOSFET according to claim 16, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

29. The power MOSFET according to claim 17, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.

30. The power MOSFET according to claim 20, wherein an impurity concentration of the epitaxial layer intervening between the trenches is set at $1 \times 10^{15}/cm^3$ or less.